REMARKS

Claims 1-42 are pending in the application. The Examiner rejects claims 1, 3-4, 6, 11, 13-22, 25-26, 28-32, 34-38, and 40-42 under 35 U.S.C. 102(b) as being anticipated by U.S. patent number 5,731,843 to Cappels Sr. The Examiner rejects claims 5, 12, 27, and 39 under 35 U.S.C. 103(a) as being unpatentable over Cappels.

The Applicants amend claims 1, 4, 6-9, 11, 13-20, 22-23, 25-26, 28-32, 36, and 42. Claims 1-42 continue to be pending in the application.

The Applicants add no new matter and request reconsideration.

Claim Rejections – 35 U.S.C. § 102 and § 103

The Applicants traverse the Examiner's claim rejections in their entirety.

Claim 1 recites an edge detector circuit to generate an edge pulse signal ... *responsive to a pixel clock*. Claims 18 and 31 include a similar limitation. The Examiner alleges Cappels discloses the recited edge detector as "the differentiator 52 [sic] and the threshold detector 44." As the Examiner points out, Cappels discloses that the "differentiator 42 and the threshold detector 44 function together to detect voltage transitions between pixel instructions...in a video signal 52. Cappels, column 4, lines 41-44. But neither Cappels' differentiator 42 nor threshold detector 44 operates responsive to a pixel clock as recited (the pixel clock is presumably at the output of the phase adjuster circuit 50).

And claim 1 recites a phase detector circuit to generate a phase adjust signal *responsive to a phase of the phase locked loop clock* and the edge pulse signal. Claim 18 includes a similar limitation. The Examiner alleges Cappels discloses the recited phase detector as "the phase comparator 46 and the microprocessor 48." But neither the comparator 46 nor the microprocessor 48 operates responsive to *a phase of the phase locked loop clock* as recited (the phase locked loop clock is presumably at the output of the pixel clock block 55).

Claim 31 recites *generating a plurality of clock phases by delaying a phase locked loop clock signal by a plurality of delays*. Cappels does not disclose that the output of the pixel block 55 is delayed *by a plurality of delays* as recited.

For these and other reasons, the Applicants believe claims 1-42 are useful, novel, and not obvious over the prior art of record.

Conclusion

The Applicants request reconsideration and allowance of claims as amended. The Applicants encourage the Examiner to call the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Graciela G. Cowger
Reg. No. 42,444

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613
Customer No. 20575

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306, on March 3, 2004.

Beth A. Nichols